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Patentanmeldung Nr. | Patent application No. | Demande de brevet n°

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Der Präsident des Europäischen Patentamts;
Im Auftrag

For the President of the European Patent Office

Le Président de l'Office européen des brevets
p.o.

R C van Dijk

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(Falls die Bezeichnung der Erfindung nicht angegeben ist, siehe Beschreibung.
If no title is shown please refer to the description.
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Metal bump with an insulation for the side walls and method for fabricating

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DESCRIPTION

METAL BUMP WITH AN INSULATION FOR THE SIDE WALLS AND METHOD FOR FABRICATING

The invention relates to a metal bump on an IC with an insulation for the side walls. The invention relates especially to a driver IC for a Liquid Crystal Display (LCD) module that is attached to a glass panel. The invention also relates to a method for fabricating a chip comprising such a bump.

Anisotropic Contact Films (ACF) is a common material for attaching the chip to the glass panel. It is an adhesive film consisting of dispersed, microscopic, electrically conductive particles 3-15 μm in diameter and an adhesive 15-35 μm thickness. A limitation of the ACF assembly technique is due to the fact that the probability of shorts between adjacent bumps increases rapidly by decreasing the gap between them. The formation of chains of conductive balls touching the side walls of two adjacent bumps may short them together. The ACF assembly technique is specially used for Chip On Glass (COG) and Chip on Foil (COF) advanced packaging applications.

US patent application US 2002/0048924 A1 discloses metal bumps that comprise at least a first metal bump having a first side wall, the first side wall comprising a first predetermined area; and at least a second metal bump having a second side wall, the second side wall comprising a second predetermined area adjacent to the first predetermined area; wherein at least the first predetermined area is covered with an insulated layer. The insulating layer may cover the entire side wall of both the first and the second metal bump. Predetermined portions of the first metal bump may be covered with an insulating layer. This results in preventing electrical shorts caused by the conductive particles. In US 2002/0048924 A1 it is disclosed to use a silicon-oxide (SiO2) or silicon-nitride (Si3N4) as material for the insulating layer on the side walls.

US patent 6,232,563 B1 concerns a connector structure for connecting a semiconductor device to an external terminal using an adhesive material including a plurality of

conductive elements. The connector structure includes a pad over the device's substrate, an electrically conductive bump over the pad connected to the external terminal's pad using a conductive adhesive material comprising a plurality of conductive elements and an insulating layer on a side surface of the electrically conductive bump, the insulating layer substantially covering an entire side surface of the electrically conductive bump to prevent an electrical short through the side surface. The disclosed method for fabricating such a connector structure comprises the steps of

i. forming a pad of a conductive material such as aluminium on a substrate on which a driving device is formed,

ii. forming a passivation layer such as a silicon oxide layer or silicon nitride layer on the overall surface of the substrate including the pad,

iii. selectively etching the passivation layer to expose a portion of the pad such that a portion of the passivation layer covers the edge of the pad,

iv. depositing a barrier layer (for example, TiW/Au, Ti/PtAu) on the exposed portion of the pad and a passivation layer,

v. selectively forming a photo resist pattern on the barrier metal to expose a portion of the barrier metal on the pad,

vi. forming a bump of gold (Au) on the barrier metal by electroplating using the photo resist pattern,

vii. removing the photo resist pattern,

viii. selectively etching the barrier metal to form a diffusion stop portion,

ix. carrying out a heat treatment,

x. forming an insulating layer, such as a polymer, photosensitive polymer, or silicon nitride layer on the bump, the passivation layer and the exposed portion of the diffusion stop portion through chemical vapor deposition (CVD), physical vapor deposition (PVD) or coating, for example,

xi. coating a photo resist on the insulating layer and

xii. selectively removing the photo resist to form a photo resist pattern defining a contact region on the bump,

xiii. etching the insulating layer using the photo resist pattern as a mask or by photo process (in the case of a photosensitive material),

xiv. removing the photo resist pattern to complete the bump electrode.

The method proposed in US 6,232,563 B1 requests a mask step where a photo resist is coated on the insulating layer and selectively removed to form a photo resist pattern defining a contact region on the bump where the insulating layer is portionally etched. Then the photo resist pattern is removed.

It is object of the invention to further develop the method for fabricating a bump according to the generic introduction. It is another object of the invention to provide a connector that is fabricated in an improved manner. It is a further object of the invention to provide metal bumps that can be easily fabricated.

As regards the method the object is solved by a method as described in claim 1. The deposited metal layer covering the chip's passivation layer and the metal pads serves as an etch stop during the etching of the insulating layer plasma. The insulation layer is deposited in a low pressure plasma activated gas where the molecules are split up into ions and electrons facilitating the reaction and increasing the deposition rate. Subsequently the use an special method based on RIE (Reactive Ion Etching) for removing the predetermined (horizontal regions on the IC surface) portions of the insulation layer simplifies the method for fabricating the chip and does help to reduce costs and processing time as those mask steps comprising the steps of (xi.) coating a photo resist on the insulation layer, (xii.) selectively removing the photo resist to form a photo resist pattern defining a contact region on the bump and (xiv.) removing the photo resist pattern to complete the bump electrode are dropped.

As regards the connector, the object is solved by a connector as described in independent claim 2. The low pressure chemical vapor deposition (LPCVD) is a process whose reaction velocity is kinetically controlled, which means that the reaction velocity is temperature-dependent. This process enables the formation of layers that

have a uniform layer thickness on horizontal regions and vertical walls of the IC surface topography. The insulation layer may be formed of silicon dioxide (SiO_2) which is formed by a reaction of silane (SiH_4) or dichlorosilane (SiH_2Cl_2) with an oxidising agent such as NO or N_2O_4. The reaction takes place in the temperature range between 430° and 633°C at a pressure of approximately 1 mbar. The activation energy of the reaction with N_2O_4 is 0.91 eV/molecule, which corresponds to 87.4 kJ/mol. This temperature range makes the method suitable for the application of a SiO_2-layer on glass, aluminium and many metal-silicides.

As regards the metal bumps the object is solved in that the insulation layer of at least two opposite side walls of two metal bumps is formed by a dielectric layer which is deposited by plasma and etched back in an anisotropic plasma etcher. The anisotropic plasma etcher can immediately be used without performing a mask step.

According to one embodiment, the dielectric material forming the insulation layer is part of the group including SiO_2 or Si_3N_4. These dielectric materials are proven for the LPCVD-process.

According to another embodiment the metal bumps are formed of a noble metal or an oxidation resistance material such as gold (Au) or a metal of the platinum group. The use of a noble metal for the bump results in a surface for the contact with the electrical conductive elements (or particles) in the ACF polymer that has a low electrical resistance.

The invention will now be described in detail with reference to the accompanying drawings where

Figure 1 shows processing steps in a cross sectional view and

Figure 2 shows a cross sectional view of a connector.

Figure 1 shows processing steps in a cross sectional view. Figure 1a) shows metal pads 1a, 1b which are added to the chip's substrate 2. A passivation layer 3 is disposed on

those portions of the substrate 2 which are not covered by any of the metal pads 1a, 1b and covers the edges of those metal pads 1a, 1b. An under bump metal layer 4 covers the passivation layer 3 and those portions of the metal pads 1a, 1b which are not covered by the passivation layer 3.

Figure 1b) shows the next step with a photo resist coated on the barrier metal 4 and selectively removed to form a photo resist pattern 5 such as to expose a portion of the metal barrier 4 over the pads 1a, 1b.

Figure 1c) shows bumps 6a, 6b formed on the exposed portions of the barrier metal 4 that are deposited using the photo resist pattern.

In Figure 1d) the photo resist pattern 5 is removed and an insulation layer 7 is deposited on the top and the side surfaces of the bump as well as on the under metal barrier 4. The insulating layer 7 is deposited in the plasma state of aggregation where the molecules are split up into ions and electrons.

Figure 1e) shows the status after performing a reactive plasma etching. Those portions of the metal layer 4 which are exposed between the side walls are removed. The insulation layer covering the vertical walls of the bump remain because of the anisotropic character of the RIE process. The remaining portions of the metal layer 4 form a diffusion stop barrier 4'.

Figure 2 shows a cross sectional schematically view of the invention connector with the bumps 6a, 6b being electrically connected with the electrode pads 8a, 8b on the opposite substrate 9.

CLAIMS

1. Method for fabricating a chip side walls with the chip comprising
   - a nonconducting substrate (2),
   - metal pads (1a, 1b) deposited on the nonconducting substrate (2),
   - a passivation layer (3) covering the nonconducting substrate (2) and the edges of the metal pads (1a, 1b),
   - a metal diffusion stop barrier (4') covering a portion of the chip's passivation layer (3) and the metal pads (1a, 1b),
   - a photo resist pattern a metal layer (4) to expose a portion of the barrier metal on the pad (1a, 1b) that is removed after use and
   - at least one bump (6a, 6b) formed of gold (Au) on the exposed portion of the pad (1a, 1b) and the edges of the metal layer (4)

   characterised by the steps of
   - depositing the metal layer (4) covering the chip's passivation layer (3) and the metal pads (1, 1b),
   - depositing an insulation layer (7) in a plasma activated reactor,
   - removing predetermined portions of the insulation layer (7) by reactive ion etching and
   - portionally removing the metal layer (4) to form the bump diffusion stop barrier (4').

2. A connector (10) comprising:
   - a plurality of electrode pads (8a, 8b) over a substrate (9);
   - a plurality of electrically conductive bumps (6a, 6b) over the substrate (2) each of the electrically conductive bumps (6a, 6b) being electrically connected to a respective one of the plurality of electrode pads (8a, 8b);

- a plurality of conductive particles on respective top surfaces of the electrically conductive bumps (6a, 6b) electrically connecting respective electrically conductive bumps (6a, 6b) to a plurality of electrode pads (8a, 8b), and
- an insulating layer (7) formed of a nitrate or an oxide on the side surfaces of each of the plurality of electrically conductive bumps (6a, 6b) to prevent an electrical short
- characterised in that the insulation layer (7) is provided by a LPCVD-process.

3. Metal bumps (6a, 6b) that comprise side walls with an insulation layer (7) on at least two opposite side walls, characterised in that the insulation layer (7) is formed by a dielectric layer which is deposited by plasma and etched back in an anisotropic plasma etcher.

4. Metal bumps as claimed in claim 3, characterised in that the dielectric material is part of the group including SiO_2 or Si_3N_4.

5. Metal bumps as described in claim 3 or 4, characterised in that the metal bumps (6a, 6b) are formed of a noble metal or an oxidation resistance material such as gold.

6. Use of a metal bump (6a, 6b) that is portionally covered with an insulation layer (7) which is deposited by a LPCVD-process for a Chip on Glass or a Chip on Foil packaging application.

ABSTRACT

METAL BUMP WITH AN INSULATION FOR THE SIDE WALLS AND METHOD FOR FABRICATING A CHIP

A chip with at least two metal bumps (6a, 6b) which has insulation layers for opposing side walls which are deposited in a plasma activated gas. Predetermined portions of the insulation layer (7) are removed by reactive ion etching. The metal bumps can be formed of a noble metal and the insulation layer of a dielectric material such as SiO_2 or Si_3N_4.

(Fig. 1e)

Fig. 1a

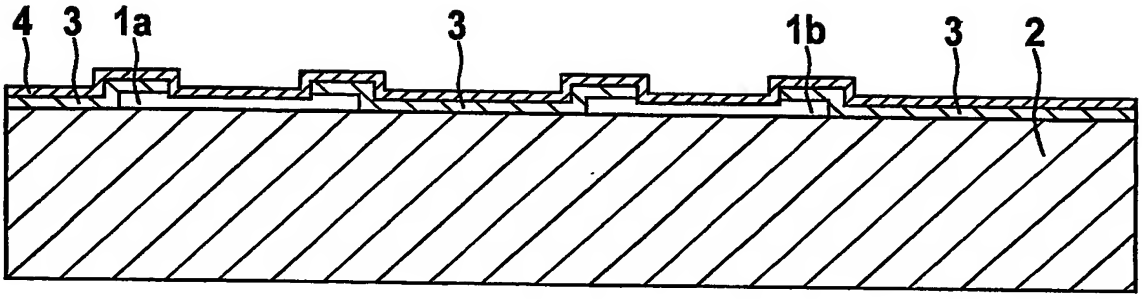


Fig. 1b

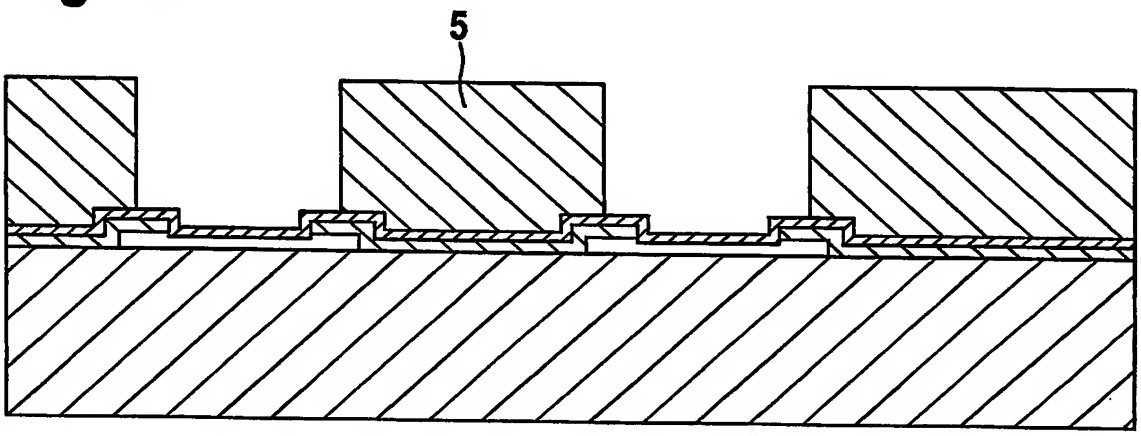


Fig. 1c

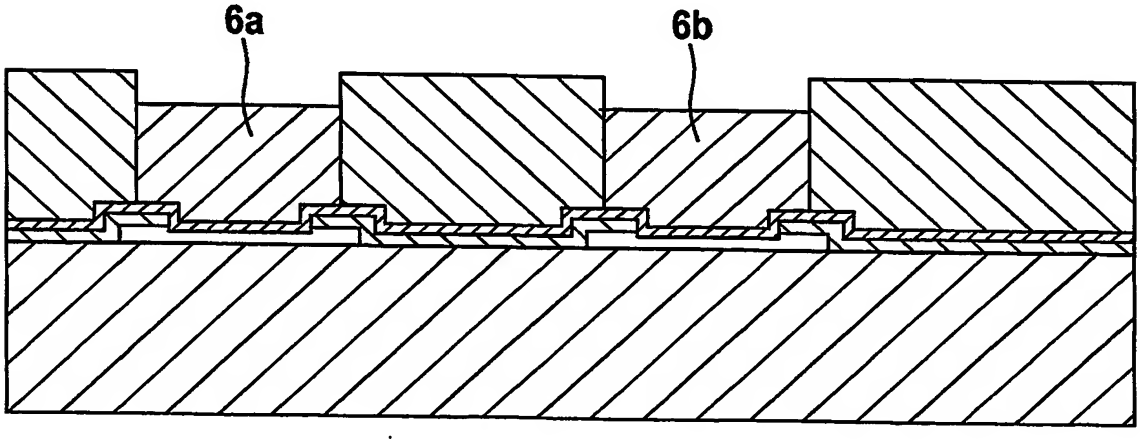


Fig. 1d

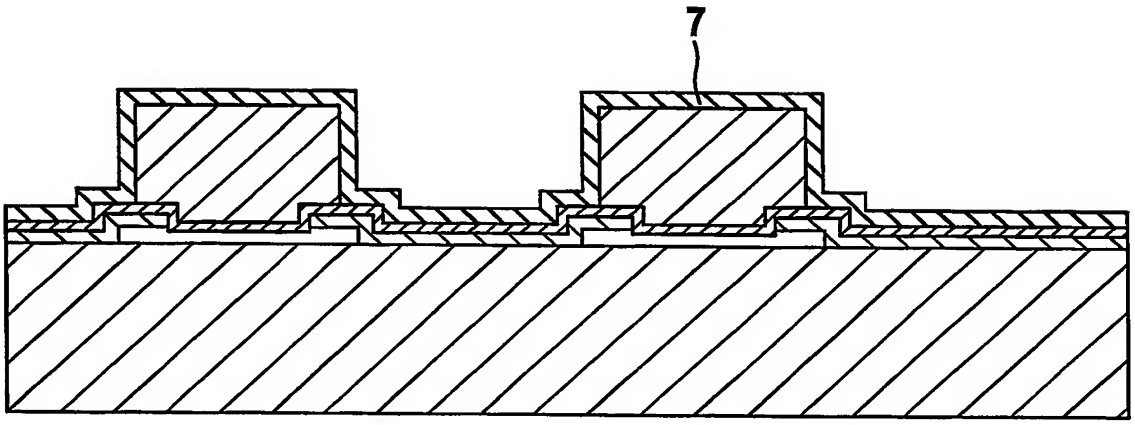


Fig. 1e

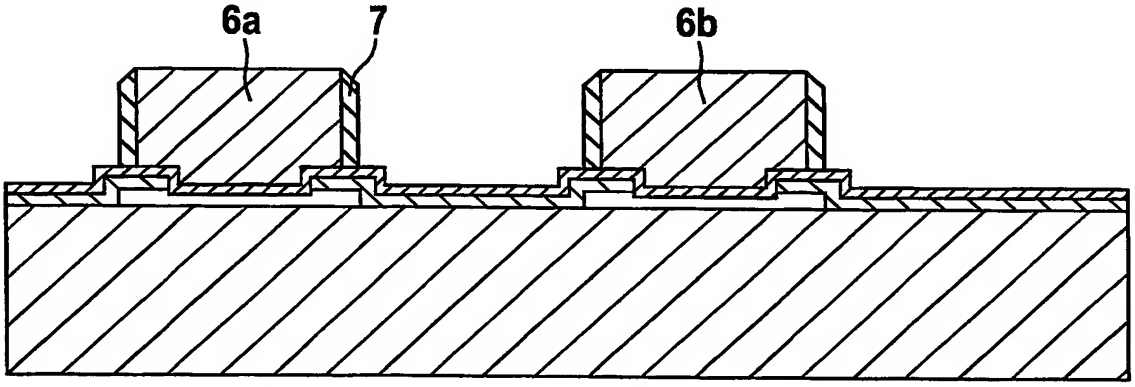
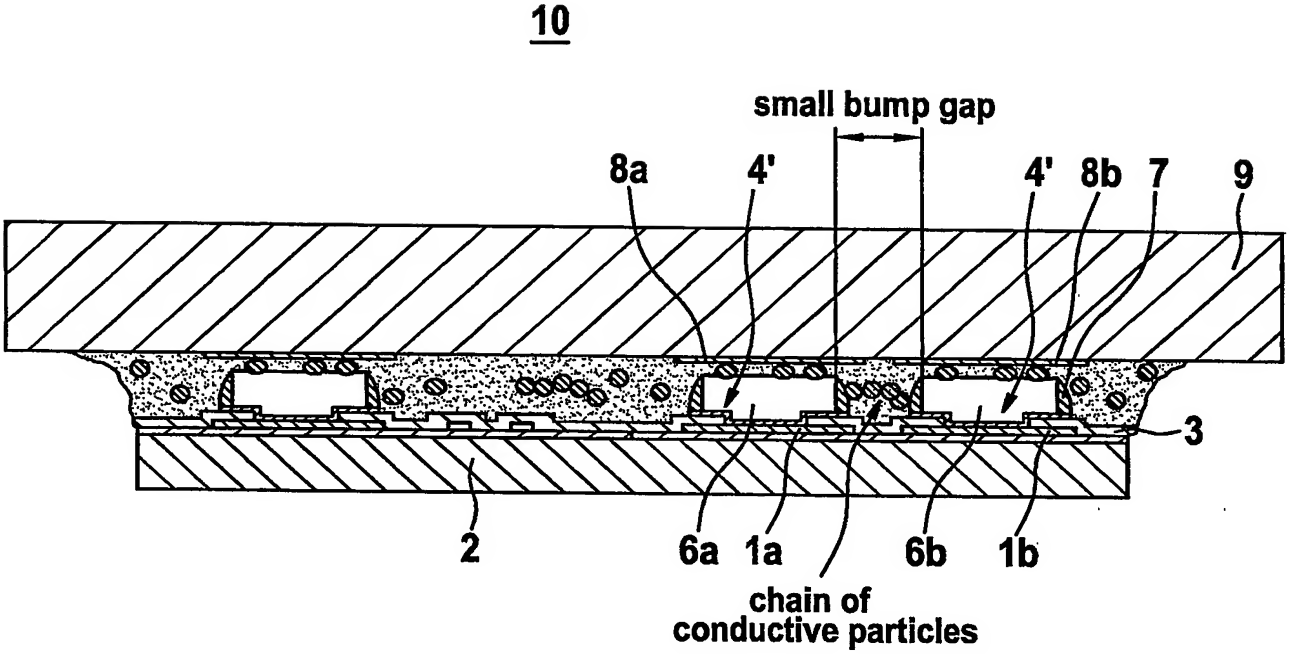


Fig. 2


10
small bump gap
8a
4'
4'
8b
7
9
3
2
6a
1a
6b
1b
chain of
conductive particles